HIGH PHASE ACCURACY ACTIVE PHASED ARRAY MODULE FOR MULTI-FUNCTION RADARS

C.J.Ward, J.R.Forrest, P.Malamis, A.A.Salles
Microwave Research Unit,
University College London,
Torrington Place,
LONDON WC1E 7JE, U.K.

M.E.Brinson, A.J.Parsons
Department of Electronics
and Communications Engineering,
Polytechnic of North London,
Holloway, LONDON N7 8DB, U.K.

The paper describes an S-Band (2.7-3.1GHz) transmit/receive phased array module giving 40W output for 100μs pulses at 10% duty cycle. The module incorporates closed-loop phase control to reduce to a low level any phase errors between the input reference signal and the output. Initial work on the development of a fibre optic interface for input of the coherent r.f. reference signal is also described.

Introduction

Recently there have been very important developments in advanced radars operating at frequencies around 1GHz. The AN/TPS-59 and GE592 have shown the viability of a solid-state approach to r.f. power generation on a modular basis. For many applications, notably in the marine environment, a higher frequency is to be preferred; it is clear that if solid-state r.f. power generation at around 3GHz can be demonstrated with the same effectiveness as has been achieved at the lower frequency, many benefits will result, particularly for shipborne and more compact multi-function phased array radars. It is to that application that the present work is primarily addressed.

Module Specification

The typical requirement for a multi-function phased array module is taken as a power output in the region of 50W for long pulses of 100μs at 10% duty cycle. Pulse compression would be used in the receiver to give adequate range resolution. Pulse-to-pulse frequency agility over some 10% bandwidth would be required and in the present work the frequency range 2.7-3.1GHz has been chosen. Two philosophies exist as regards phase control in array modules. The insertion phase of a module can be allowed to have a wide tolerance, which is then calibrated out during installation or by external monitoring. Alternatively, the insertion phase may be constrained to very tight tolerances with the aim of simplifying installation, replacement or monitoring procedures. This latter technique has been adopted in the present work, the aim being to provide an insertion phase error, from module to module, not exceeding approximately 1^{0}, even during the r.f. pulse.

Module Configuration

Possible configurations for active phased array modules have been described by Austin and Forrest [1]. The straightforward amplifier approach (Fig.1) suffers from the disadvantage of many amplifier stages with attendant cascading of insertion phase errors from each stage, and from the need for r.f. phase shifters which are generally rather inaccurate. The phase locked loop approach (Fig.2), however, offers the possibility of fewer amplifier stages, dynamic control of phase errors even during the output pulse, and phase shifting at intermediate frequency.

Transmit Section

The basic configuration chosen uses the heterodyne phase locked loop approach as shown in Fig.3.

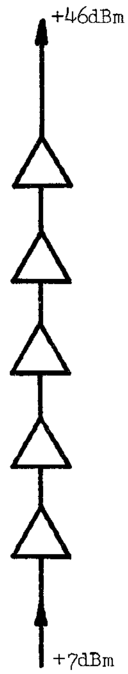

Fig.1: Amplifier Approach to Module Design

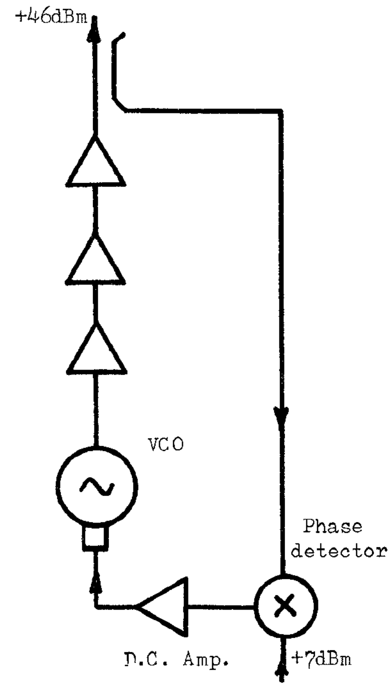

Fig.2: Phase Locked Loop Approach to Module Design

A pulsed voltage-controlled oscillator (VCO), tunable over 2.7-3.1GHz provides in excess of +20dBm through an isolator to a buffer amplifier (TRW 54601). The output of this stage provides the +25dBm drive to a line-up of three Class C power amplifier stages (TRW CTX 1191-2-3) with a final output power of approximately 40W. Each stage has some 7dB of gain and these transistors have particularly high collector efficiency (∿45%) which keeps thermal power dissipation in the module to an acceptable level. The final output power passes through a four-port circulator which provides mismatch protection for the output transistor against large reflections from the antenna or the limiter in the receive channel. On the output line, a -30dB coupler samples the output signal which, after a further 10dB of attenuation, is fed to a single balanced r.f. mixer; the mixer takes the coherent array reference signal at +7dBm as a local oscillator drive and downconverts the sampled transmitter output to i.f. This downconverted signal is taken directly to an i.f. mixer (WJ M6D) acting as a phase detector; the phase reference is provided by an external 70MHz signal carrying the required phase information for the transmit r.f. output. The phase detector output is amplified in a very fast d.c.-coupled amplifier and fed to the varactor of the VCO. Phase locking of the output to a frequency equal to the sum of the r.f. and i.f. reference frequencies is obtained by a simple programmed pretuning of the VCO to within the first-order capture range of the loop; if required, the system can be programmed to lock on the difference of r.f. and i.f. reference frequencies.

0149-645X/82/0000-0179 $00.75

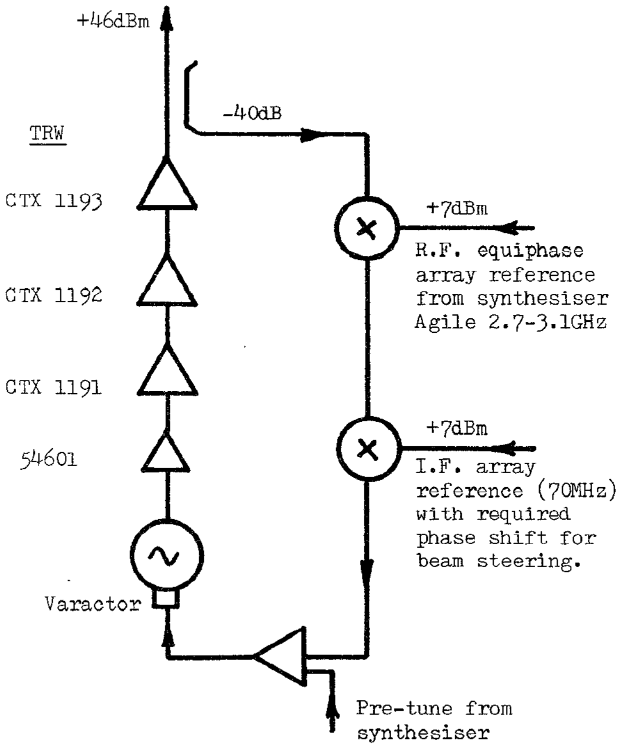

Fig.3: Heterodyne Phase Locked Loop Module

The main disadvantage of a phase locked loop approach is that, unless some output signal gating is used, the loop locking transient is part of the radiated r.f. pulse. It is thus important that this lock-up period, during which the output frequency and phase are uncontrolled, should be as small a fraction of the total pulse duration as possible. A major part of the effort in the module development has therefore been devoted to the achievement of very fast lock-up. Conventional thick-film or integrated circuit d.c. amplifiers for providing the loop gain have high values of delay (many ns) and it was necessary to design a new type of loop amplifier (tandem amplifier) in which high frequency and low frequency components of the loop signal are separately amplified and combined before being applied to the varactor. This gives a group delay less than 1ns for the high frequencies and results in very fast first-order capture characteristics; at marginal stability the loop capture range is approximately 100MHz, but this reduces to 25MHz when an adequate loop stability margin ($\sim$10dB) is allowed, giving a lock-up time of a few tens of ns. This 25MHz capture range is needed to take account of long-term drift of free-running frequency of the VCO such as occurs with temperature variations. The low frequency path in the loop amplifier provides a gated integrator action to reduce the phase error between the output and the input reference to a very low value soon after the start of the pulse.

Another critical component in the module is the VCO. To avoid the need for many following amplifier stages, the VCO output power should be as high as possible; there is a trade-off between power output and electronic tuning range, however, due to rectification effects in the varactor. The present design uses a silicon bipolar transistor (Mullard M01B) in a microstrip circuit giving a power output in excess of +20dBm. Electronic tuning is accomplished, with the high linearity needed (Fig.4) to ensure a constant stability margin, by means of a hyperabrupt GaAs varactor (MA 46628).

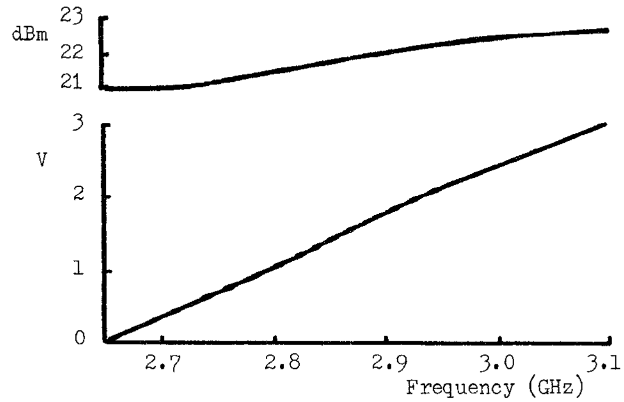

Fig.4: VCO Power Output and Tuning Characteristic with Varactor Voltage

Receive Section

After passing through the four-port circulator and a limiter, the received signal is amplified by a conventional low-noise amplifier using a silicon bipolar transistor (HXTR 6101), giving some 11dB of gain over the frequency band. Downconversion to a 70MHz i.f. is accomplished in an image-rejection mixer (20dB rejection) using Si beam lead diodes, followed by 10dB of i.f. amplification to drive the module i.f. output line. The overall noise figure of the receiver is close to 5dB.

Circuit Technology and Overall Assembly

The module is constructed around a hollow 2"x1"x 12" rectangular tubular backbone. This provides a channel for blown air cooling when modules are densely packed in an array environment. The microwave circuits are laid out on 0.040" thick 2"x2" or 2"x1" alumina or ferrite substrates using thick-film fritless Pd-Ag ink technology. Only the VCO and i.f. amplifier boards use low dielectric constant 'RT Duroid' substrates. The transmit section is mounted on one side of the backbone and the receive side on the other; all substrates have a thick-film metallised ground plane and are mounted on to the backbone with indium shims.

A photograph of the module (receive side) is shown in Fig.5. Six modules are being constructed to assess aspects of quantity production, reapeatability of performance and test procedures.

Module Performance

The power output over the frequency band is shown in Fig.6. Typical lock-up performance is shown in Fig.7 from which it is seen that the main part of the locking transient is over within 50ns and that the phase has settled to within a few degrees of the final value after 150ns. Without the phase locked loop control, some 30^{o} of total phase variation during the pulse occurs from the power transistor line-up and several MHz of chirp occurs in the VCO. The output spectrum shows excellent fidelity to sin(x)/x form and spurious signals are all below -55dBc. Droop on the output power pulse is 0.2dB and this is highly dependent on the amount of power supply storage capacitance in the module; at present, each transistor has a 20μF tantalum capacitor close to the bias network and there is a 4700μF electrolytic capacitor for the module as a whole. The module operates from +26V and -24Vd.c. supply lines, overall d.c. to r.f. efficiency being $\sim$26%. Elimination, or pulsing, of the Class A stage on the transmit side would raise efficiency to 30%.

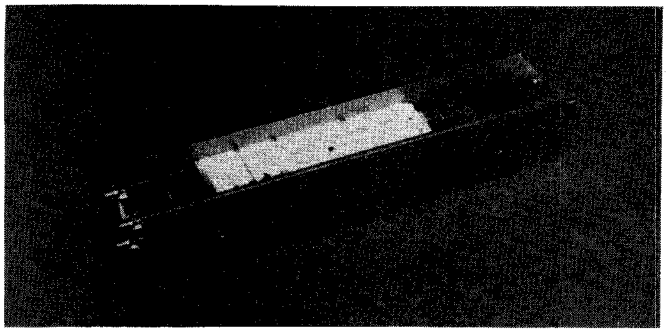

Fig.5: Photograph of the Module (Receive Side).

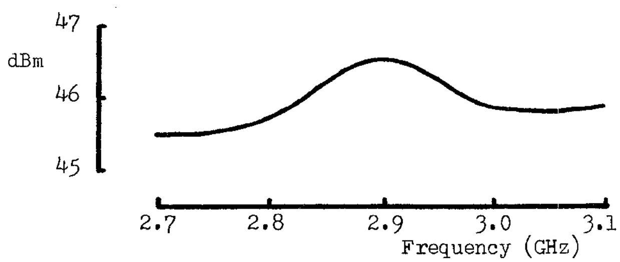

Fig.6: Module Output Power Variation over the Band.

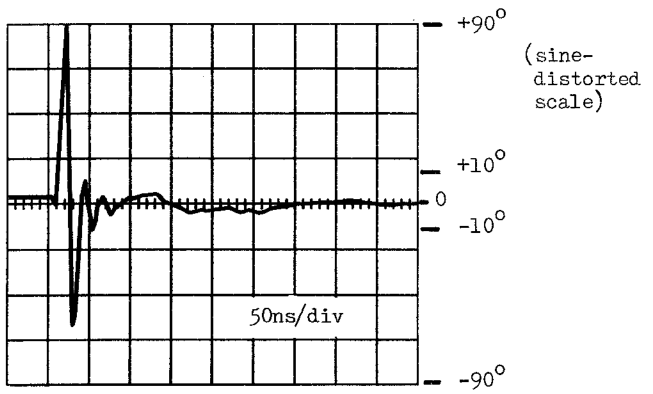

Fig.7: Output Phase Variation at the Start of the R.F. Pulse, showing the Lock-up Transient.

Optical Control of the Module

Future developments in phased array modules will undoubtedly involve greater use of monolithic chips, simplifying module construction[3] and placing greater attention on the problems of distributing phase coherent references and control signals to the array. A start has therefore been made towards the goal of a module which has all reference and control inputs on a single optical fibre. Technology and techniques for the modulation, transmission and detection of i.f. (70MHz) and digital signals on an optical carrier may be realised using commercially-available, low-cost components. The most difficult problem is the coherent r.f. reference distribution and this has been investigated first.

The scheme uses the optical injection locking principle [4](Fig.8). A coherent microwave reference signal at 2.8GHz amplitude modulates a GaAlAs laser (ITT LS7709) which has a single-mode optical output of 5mW at 0.85μm wavelength. Up to 100% modulation depth can be achieved with only a few mW of useful microwave drive power, but coupling of the microwave drive power to the laser is currently inefficient and some 100mW of power is used from the reference source. The modulated laser output, after transmission through a short length of fibre or a free-space path, is demodulated by focussing it on to the gate region of a microwave MESFET (Plessey GAT6) in an amplifier or oscillator circuit tuned to a frequency close to that of the modulation. Optical coupling to the MESFET is also at present very inefficient, but the few μW of received optical power are adequate to injection lock such a MESFET oscillator over a few MHz locking range [5]. In the present experiments, the locked oscillator output level is of the order of +3dBm which, after amplification in the second MESFET, provides the +13dBm for the module phase locked loop reference mixer and the receiver image rejection mixer. The reference signal obtained at the module shows noise performance similar to that of the laser modulation source.

The scheme has only been used at one microwave frequency since the optical locking range is insufficient for much frequency agility. However, improved optical coupling and pretuning of the MESFET oscillator are likely to provide a fully frequency-agile system. The present work shows that optical distribution of the array reference signal is a viable proposition and only requires optical signals at the μW level, an important feature if many array elements are to be supplied from a single laser.

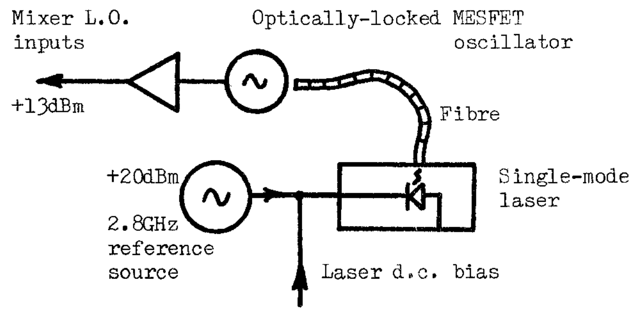

Fig.8: Arrangement for Optical Interface with the Module for R.F. Reference Signal Input.

Acknowledgement

The authors gratefully acknowledge research grants from the U.K.Ministry of Defence, P.E.(Admiralty Surface Weapons Establishment) and the United States Air Force Office of Scientific Research (Rome Air Development Center, Hanscom AFB). Assistance in the provision of MESFETs for the optical control experiments has been received from Plessey Research (Caswell) and thanks are extended to Mr R. Pengelly.

References

1. Austin,J and Forrest,J.R.:'Design concepts for active phased array modules'. IEE Proc, 127, Part F, No.4, pp.290-300 (1980).
2. Ward,C.J.:'Delay reduction techniques in phase locked loop amplifiers'. Electronics Letters, 17, No.7, pp.253-255 (1981).
3. Forrest,J.R.:'Phased arrays - current technology and future prospects'. Proc. 11th. European Microwave Conference, Amsterdam, 1981, pp.81-90.
4. Forrest,J.R. and Salles,A.A.:'Optics control microwaves'. Micr.Sys.News, 11, No.6, pp.112-122 (1981).
5. Salles,A.A. and Forrest,J.R.:'Initial observations of optical injection locking of GaAs MESFET oscillators'. App. Phys. Lett., 38, pp.393-393, (1981).